Comparison of Three SVPWM Strategies

Wei-Feng Zhang and Yue-Hui Yu

***Abstract*—Three space vector pulse width modulation (SVPWM) schemes, called 7-segment space vector modulation (SVM), 5-segment SVM and 3-segment SVM are studied in this paper. The basic principle of SVPWM is presented. The switching sequence of different scheme is described. The modulation signals, DC bus voltage utilization, and output line voltage harmonic of these schemes are analyzed by the MATLAB software with different modulation index *M* and frequency modulation index *N*. The simulation results are analyzed and show that discontinuous modulating functions lead a reduction of switching actions. The DC bus voltage utilization of three schemes is almost the same. For all three SVM, the frequency modulation index *N* will affect the harmonic characteristic, and the modulation index *M* will affect DC bus voltage utilization and the harmonic content. The experiment is implemented by the DSP of TMS320F2812. The results validate three algorithms and the simulation.**

***Index Terms*—DC bus voltage utilization, harmonic, switching loss, switching sequence, space vector pulse width modulation.**

1. Introduction

Space vector pulse width modulation (SVPWM) technique is widely used in inverter and rectifier controls [1]-[5]. Compared to the sinusoidal pulse width modulation (SPWM), SVPWM is more suitable for digital implementation and can increase the obtainable maximum output voltage with maximum line voltage approaching 70.7% of the DC link voltage (compared to SPWM's 61.2%) in the linear modulation range. Moreover, it can obtain a better voltage total harmonic distortion factor.

There are different algorithms for using SVPWM to modulate the inverter or rectifier. Many SVPWM schemes have been investigated extensively in literatures [6]-[9]. The goal in each modulation strategy is to lower the switching losses, maximize bus utilization, reduce harmonic content, and still achieve precise control. So the performance of a SVPWM scheme is usually judged based on the following criteria[10]: total harmonic distortion (THD) of output voltages, switching losses of inverters, and maximum output voltage. For these criteria, the modulation signals, DC bus voltage utilization, and output line voltage harmonic are the main evaluated objects.

In this paper, three space vector modulation (SVM) schemes are investigated. The modulation signals, DC bus voltage utilization, and output line voltage harmonic are analyzed with different modulation index *M* and frequency modulation index *N*. In addition, the experiment is implemented by the DSP of TMS320F2812.

2. Principles of SVPWM

SVPWM is based on the fact that there are only two independent variables in a 3-phase voltage system. We can use orthogonal coordinates to represent the 3-phase voltage in the phasor diagram. A three-phase-voltage vector can be expressed as:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} v_{\mathrm{AO}} \\ v_{\mathrm{BO}} \\ v_{\mathrm{CO}} \end{bmatrix} \quad (1)$$

In the SVPWM scheme, the 3-phase output voltage is represented by a reference vector which rotates at an angular speed of $\omega=2\pi f$. The task of SVM is to use the combinations of switching states to approximate the reference vector, $\mathbf{V}_{\mathrm{ref}}$. To approximate the locus of $\mathbf{V}_{\mathrm{ref}}$, the eight possible switching states of the inverter are represented as 2 null vectors and 6 active vectors. The operating states and corresponding vectors are listed in Table 1.

Table 1
Switching states of the 2-level inverter

Space vector		Switching state	'On' switches S_i
Zero vector	$\mathbf{V}_7$	[111]	1, 3, 5
	$\mathbf{V}_0$	[000]	4, 6, 2
Active vector	$\mathbf{V}_1$	[001]	4, 6, 5
	$\mathbf{V}_2$	[010]	4, 3, 2
	$\mathbf{V}_3$	[011]	4, 3, 5
	$\mathbf{V}_4$	[100]	1, 6, 2
	$\mathbf{V}_5$	[101]	1, 6, 5
	$\mathbf{V}_6$	[110]	1, 3, 2

These vectors ($\mathbf{V}_1$~$\mathbf{V}_6$) can be used to frame the vector plane, which is illustrated in Fig.1.The rotating reference vector can be approximated in each switching cycle by switching between the two adjacent active vectors and the zero vectors. In order to maintain the effective switching frequency at a minimal value, the sequence of the toggling between these vectors is organized in such way that only one

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leg is affected in every step.

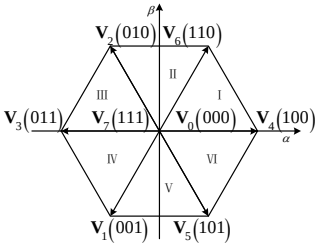

Fig. 1. Vector plane frame.

3. Three SVPWM Schemes

The sector judgment and application time of active vector for all SVM strategies are the same. So we will only describe the switching sequences of different scheme in details in this section.

The choice of the null vector determines the SVM scheme. There are a few options: the null vector $\mathbf{V}_0$ only, the null vector $\mathbf{V}_7$ only, or a combination of the null vectors.

A popular SVM technique is to alternate the null vector in each cycle and to reverse the sequence after each null vector. This will be referred to as the symmetric 7-segment technique. Fig. 2 shows conventional 7-segment switching sequences of sector I. It is shown that the sequence $\mathbf{V}_0$-$\mathbf{V}_4$-$\mathbf{V}_6$-$\mathbf{V}_7$ is used in the first $T_s/2$, and the sequence $\mathbf{V}_7$-$\mathbf{V}_6$-$\mathbf{V}_4$-$\mathbf{V}_0$ is used in the second $T_s/2$. The sequences are symmetrical. The switching frequency is the same as sampling frequency of the inverter.

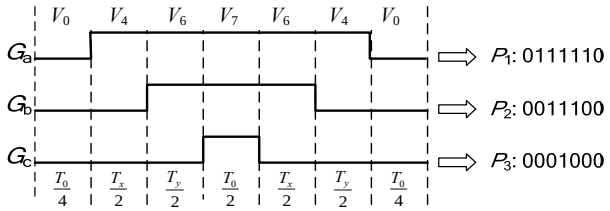

Fig. 2. Conventional 7-segment switching sequences of sector I.

Another SVM technique is referred to as 5-segment algorithm. Fig.3 shows 5-segment algorithm switching sequences of sector I. Only null vector $\boldsymbol{V}_7$ is used in each cycle. Its sequences are symmetrical too. This scheme lowers the switching times. Moreover, the algorithm can be implemented easily by DSP.

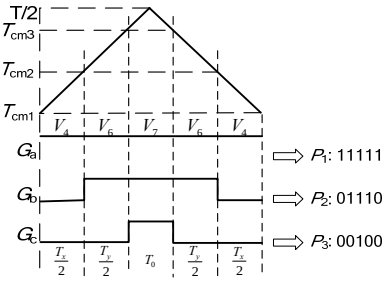

Fig. 3. 5-segment switching sequences of sector I.

Fig. 4 shows the 3-segment algorithm sequences of sector I in 2 sampling periods. This scheme is designed as follows. Assuming the reference vector located in sector I, the first sampling point uses the sequence $\mathbf{V}_4$-$\mathbf{V}_6$-$\mathbf{V}_7$, which goes counter-clockwise along the vertices of the sector, and then the next sampling point uses $\mathbf{V}_6$-$\mathbf{V}_4$-$\mathbf{V}_0$, which goes clockwise. The counter-clockwise and clockwise sequences are used alternatively. The dwelling time of each sequence is calculated at the sampling frequency. It is clear in Fig. 5 that there are only 0.5 switching action in each sampling periods; this means the sampling frequency can be doubled at a certain switching frequency. Two types of sequences, S_p and S_q, can be defined (Fig. 4), where, S_p is the P-type sequence which contains null vector PPP(111), and S_q is q-type sequence containing null vector QQQ(000). T_x (the application time of the first active vector) and T_y (the application time of the second active vector) should be swapped when the vector is located in even number sectors.

The gate sequences of 6 sectors are concluded in Table 2 for all schemes. From the Fig. 4, it is known that the switching times is lowest.

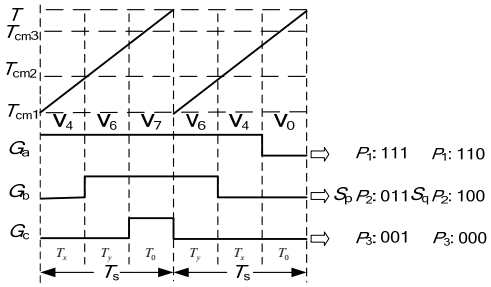

Fig. 4. 3-segment switching sequences of sector I.

Table 2
Switch sequences of the 6 sectors for all schemes

Sector	Sequences
I	$P_1P_2P_3$
II	$P_2P_1P_3$
III	$P_3P_1P_2$
IV	$P_3P_2P_1$
V	$P_2P_3P_1$
VI	$P_1P_3P_2$

4. Simulation Results

Simulink models for three algorithms were built respectively based on the above definition of switching sequences. The model was run according to the following parameters sets: DC link voltage V_d =310 V, output line voltage frequency f=50 Hz, R = 16.25Ω, L = 0.25mH.

4.1 Modulation Waveform

The modulation waveform of the 7-segment SVM strategy has the saddle shape, which is shown in Fig. 5(a) with M=1 and N=12, where M is the modulation index and N is the frequency modulation index. It is a continuous function, linearly dependent on the modulation index and symmetrical with respect to the center of the periods. The continuity of the

modulation waveform implies that in each leg of the inverter, switching occurs within all six sectors of the output voltage. And it is clear that there are 12 switching actions in each period for the classic strategy.

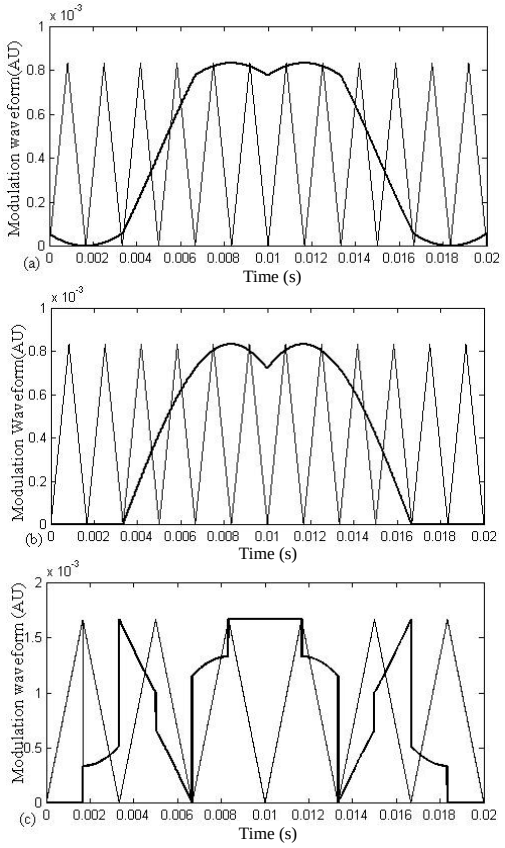

Fig. 5. Modulation waveforms of three SVPWM schemes: (a) the 7-segment scheme, (b) the 5-segment scheme, and (c) the 3-segment scheme.

Fig. 5(b) shows the modulation waveform of the 5-segment SVM. The waveform has the shape of saddle and symmetrical with respect to the center of the periods too. But it is discontinuous. It can be seen that within the total of one-third of the cycle of output voltage, the modulating waveform assumes the values of 0. Consequently, in a given leg of the inverter, switching occurs within the total of only two-thirds of the cycle and there are only 8 switching actions in each period. As a result, switching losses are significantly reduced in comparison with those in an inverter controlled by using a continuous modulating function.

Fig. 5(c) shows the modulation waveform of the minimum-loss strategy called the 3-segment SVM. Compared to the 7-segment and 5-segment SVM, it has a lower switching frequency. There are only 6 switching actions in each period. Moreover, the modulation waveform is not continuous. Fig. 5(b) and Fig. 5(c) indicate that discontinuous modulating functions lead a reduction of switching actions [7].

4.2 DC Bus Voltage Utilization

The simulation results of DC bus voltage utilization are shown in Fig. 6. Detailed analysis reveals that DC bus voltage utilization of three schemes is almost the same. So a general simulation analysis is given as follows.

The operation in the linearity region or over-modulation region is determined by the modulation factor M, which is defined as $M = \sqrt{3}\mathbf{V}_{\mathbf{ref}} / V_d$, where $\mathbf{V}_{\mathrm{ref}}$ is the reference vector and V_d is the DC link voltage.

When M=1 in the linearity region, the output line voltage value is the same as V_d as shown in Fig. 6(a). If M<1, the output line voltage is smaller than the maximum value V_d as shown in Fig. 6(b).

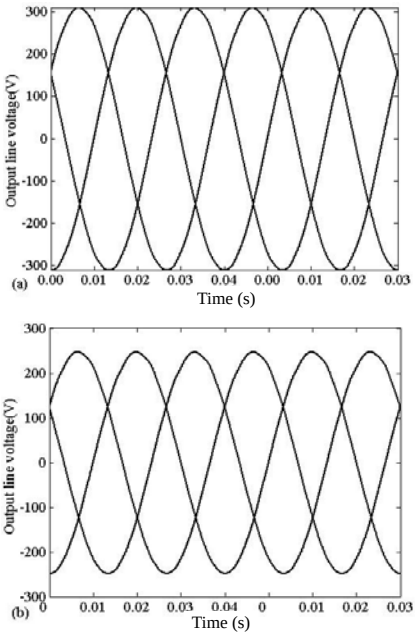

Fig. 6. Output line voltage when m≤1: (a)M=1 and (b) M<1.

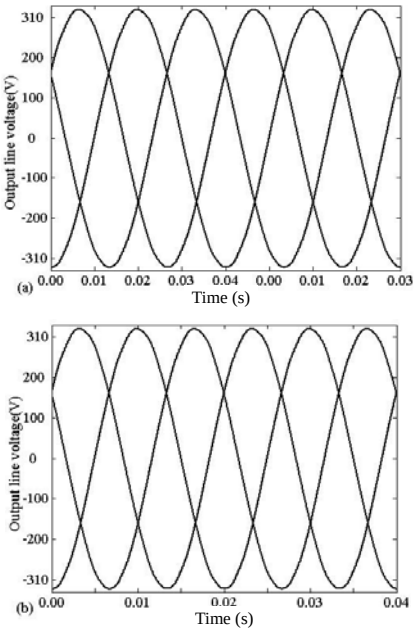

Fig. 7. Output line voltage in over-modulation region: (a) M=1.06 and (b) M=1.16.

The over-modulation region can be divided into two sections. If $V_d/\sqrt{3} \le \mathbf{V}_{\mathrm{ref}} \le (2/3)V_d$, the simulation results are

shown in Fig. 7(a). And when $\mathbf{V}_{\text{ref}} > (2/3)V_d$, the simulation results are shown in Fig. 7(b). It is shown that the maximum output line voltage could exceed the value of V_d. However, the maximum output line voltage changes little in the two sections. These results show that SVPWM can improve the DC bus voltage utilization compared to SPWM.

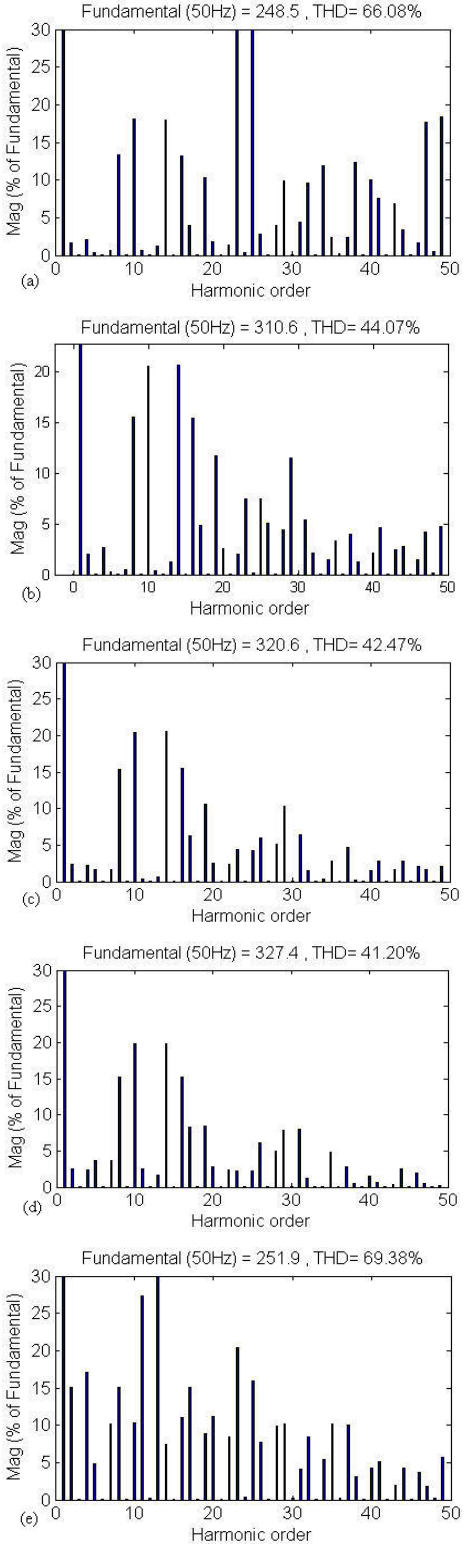

Fig. 8. Harmonics spectrum of 3-segment SVM: (a) M = 0.8 and N =24, (b) M =1and N=24, (c) M =1.06 and N=24, (d) M =1.16 and N=24, and (e) M=0.8 and N=12.

4.3 Harmonic Comparison of Three SVM

Fig. 8 shows the spectrum of the output line voltage for 3-segment SVM with different modulation indices. When the modulation index increases the THD of the output voltage decreases. In the two over-modulation regions, the THD changes little. But with the increase of M, the main harmonic region shifts to the low frequency. From Fig. 8(a) and (e), it is known that the THD decreases when N increases. These results apply to the 5-segment SVM and 7-segment SVM too. In addition, it can be seen that the fundamental voltage increases with the increase of modulation index M.

Fig. 9 shows the output line voltage spectrum of the 5-segment SVM and Fig. 10 shows the output line voltage spectrum of the 7-segment SVM. Compared to the 3-segment SVM, The THD of the 7-segment SVM is lowest under the same switching frequency and The THD of the 5-segment SVM is in-between.

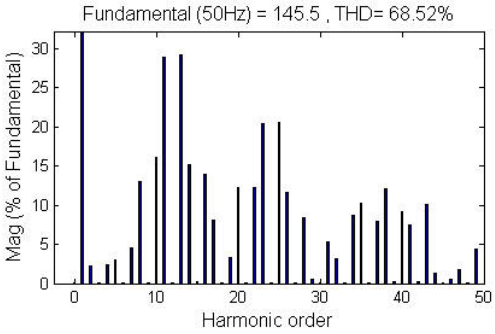

Fig. 9. Harmonics spectrum of 5-segment SVM with M =0.8 and N =12.

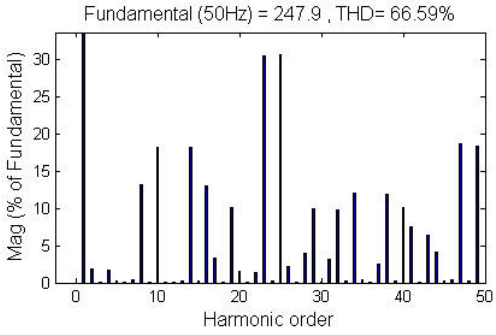

Fig. 10. Harmonics spectrum of 7-segment SVM with M =0.8 and N=12.

5. Experiment Results

By using TMS320F2812 DSP, experiments were carried out to prove the validity of three SVM. Parameters are given as follows: $M = 0.7$, $T_s = 10\ \mu s$, $T = 2$ ms (T_s–sample time, T–output voltage period).

All experimental results are shown in Fig. 11. It is clear that the 3-segment SVM has the least switching actions, the 5-segment SVM take second place and the switching actions of the 7-segment SVM are the most. These results are identical with the simulation results.

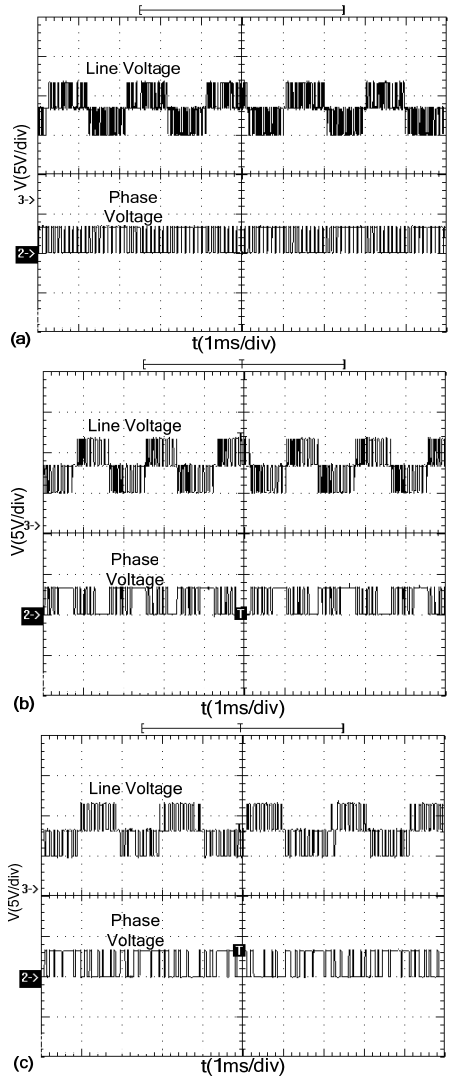

Fig.11. Experimental waveforms of DSP: (a) the 7-segment SVM, (b) the 5-segment SVM, and (c) the 3-segment SVM.

6. Conclusions

SVM is a popular choice in the inverter or rectifier controls. Three SVM schemes are presented and analyzed through simulation. The comparison study shows that all three SVM schemes can obtain almost the same output voltage in linearity modulation or over-modulation region. But the modulation waveforms are different, i.e. the modulation waveform of the 7-segment scheme is continuous and the other modulation waveforms are discontinuous. Consequently, the switching loss of the 3-segment SVM scheme is the lowest and the 7-segment SVM scheme performs better in terms of THD of the output line voltage, with the same M and N. Although the 5-segment SVM scheme performs badly in terms of the THD and switching loss, it can be implemented easily by DSP in practice. The experimental results demonstrate the validity and efficiency of three SVM schemes and the simulation.

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