Quick System-Level DDR3 Signal Integrity Simulation Research

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Abstract—Double data rate synchronous dynamic random access memory (DDR3) has become one of the most mainstream applications in current server and computer systems. In order to quickly set up a system-level signal integrity (SI) simulation flow for the DDR3 interface, two system-level SI simulation methodologies, which are board-level S-parameter extraction in the frequency-domain and system-level simulation assumptions in the time domain, are introduced in this paper. By comparing the flow of Speed2000 and PowerSI/Hspice, PowerSI is chosen for the printed circuit board (PCB) board-level S-parameter extraction, while Tektronix oscilloscope (TDS7404) is used for the DDR3 waveform measurement. The lab measurement shows good agreement between simulation and measurement. The study shows that the combination of PowerSI and Hspice is recommended for quick system-level DDR3 SI simulation.

Index Terms—Double data rate synchronous dynamic random access memory, Hspice, PowerSI, signal integrity, system-level signal integrity simulation.

1. Introduction

Synchronous dynamic random access memory (SDRAM) is widely used in computer systems to store and retrieve data. Double data rate SDRAM (DDR3) is the current mainstream memory technology used in mobile, desktop, and server market segments. DDR3 supports data rate from 800 Mbps up to 1600 Mbps[1]. With the significantly increasing signal rates and low power consumption requirements, the DDR3 design is facing more and more challenges, such as signal integrity (SI) and power integrity (PI) problems. To better resolve these problems or design bottlenecks, we need to consider all the effects from the die, package, and printed circuit board (PCB).

A lot of studies have been done about the DDR3 design, simulation, and measurement recently. A general system SI analysis methodology is to extract the equivalent models of the first-level package and various discontinuities in the PCB, and then link them together by using general transmission-line models for the interconnections[3]. The system-level PI modeling methodology in three different levels, chip, package, and PCB, for the DDR3 high-speed memory were established in [3]. Moreover, system-level SI/PI co-simulation has also been performed for a DDR3 platform in [4]. Besides this kind of system analysis, some studies that just focus on some specific structures have been conducted, e.g. signal integrity analysis of bus turn-around on a DDR3 SDRAM memory channel[5].

2. Simulation Methodology

DDR3 is so important in current system designs, while the hard situation is that there is often little time left for the SI engineer to debug or verify some SI issues before PCB tapes out. Thus, how to quickly setup a system-level SI simulation flow for the DDR3 interface is the focus of this paper.

In order to demonstrate the quick system-level DDR3 SI simulation flow, a field programmable gate array (FPGA) development board (as shown in Fig. 1) is used. This board is based on the Altera Stratix IV GX 40 nm process EP4SGX230KF40C2N FPGA, and it supports 1066 Mbps (533 MHz) DDR3 and other high-speed interfaces like peripheral component interconnect-express (PCI-E) Gen2, high definition multimedia interface (HDMI), low-voltage differential signaling (LVDS), and universal serial bus 2 (USB2). Besides the hardware system, Altera also provides a software kit called the board test system to test the functionality of the Stratix IV GX FPGA development board, which allows to read and write the DDR3 memory easily.

Generally, the system-level simulation can be performed in the frequency domain and time domain. Due to the more and more complex board topology, currently it is very hard to finish these analyses in a pure theoretical way. Fortunately, there are many commercial electronic design automation (EDA) tools that can be used here.
In frequency domain for some special 3D structures such as the via hole, connector or reference plane problems, Ansys high frequency structure simulator (HFSS) and computer simulation technology (CST) are proved good tools for the full-wave 3D electromagnetic (EM) extraction. With the significant enhancement of the computer performance, HFSS or CST can also be used for high-speed trace modeling but not recommended. For the whole system frequency-domain board modeling, considering the trade-off between accuracy and efficiency, Ansys SIWave and Sigrity PowerSI are two popular tools. These tools are 2.5-dimensional (2.5D) EM extraction tools which can finish the whole PCB $S$-parameter extraction very efficiently while keeping high accuracy. In this paper, PowerSI is chosen for PCB board-level $S$-parameter extraction.

### 2.1 Board-Level $S$-parameter Extraction in Frequency-Domain

The interested nets are routed in the the inner layer as serpentine stripline as shown in Fig. 2, where ADD is the address signal, CLK is the clock signal, DQ is the Bi-directional data, and DQS is the Bi-directional data strobe. After PowerSI simulation, the insertion loss and return loss for ADD, CLK, DQ, and DQS are shown in Fig. 3 (a) and (b). The extraction range is from DC to 6 GHz.

![Practical layout](image)

#### Fig. 2. Practical layout: (a) ADD/CLK and (b) DQ/DQS.

Fig. 3 (a) shows the ADD/CLK return loss is bigger than $-10$ dB above 500 MHz, thus its effective frequency bandwidth is only 500 MHz. So its performance is not good enough for this DDR3 working at 1066 Mbps (533 MHz). Fig. 3 (b) shows the DQ/DQS return loss is less than $-10$ dB up to 3 GHz, so its frequency performance is pretty good.

### 2.2 System-Level Simulation Assumptions in Time-Domain

For time-domain system-level simulation, Cadence SigXplorer, Synopsys Hspice, and Sigrity Speed2000 are some typical commercial EDA tools. Among them SigXplorer is applied to pre-layout SI simulation. Hspice is a good tool for both pre-layout and post-layout SI simulation, and Speed2000 is suitable for post-layout simulation. In this paper, Hspice and Speed2000 are chosen for quick system-level SI simulation.

As shown in Fig. 4, there are three main part models for a typical DDR3 system: the FPGA model, board model including single-ended or differential, and SDRAM model. In Fig. 4, TL_A, TL_B, and TL_C represent different part of transmission lines. The FPGA model is from Altera, and the SDRAM model is from Micron with different on-die termination (ODT) configurations.

For the input pattern, a K28.5 pattern is often used for a high-speed channel, which is a special character in the 8B/10B coding table. A repeating K28.5 pattern (composed of K28.5+ and K28.5−) contains five consecutive 1 and five consecutive 0, and the longest consecutive identical digits (CID) are found in 8B/10B coded data. It also contains the isolated 1—‘010’ and the isolated 0—‘101’. These characteristics make the K28.5 pattern useful for measuring the deterministic jitter. And the data pattern in simulation deck can be read from the measured waveforms.

![Waveforms](image)

#### Fig. 3. Insertion loss and return loss: (a) ADD/CLK and (b) DQ/DQS.
For the board model in Hspice, a 16 port touchstone file should be extracted with PowerSI ver11.1. For the Speed2000 flow, no board model should be extracted before simulation, for Speed2000 can extract the model automatically. In a high-speed system, electrical characteristics of the transmission lines should be strictly controlled. However, the reflection is unavoidable due to the impedance mismatch, thus overshoot or undershoot happens. The reflection coefficient $\rho$ can be calculated from (1). On the other hand, crosstalk is another important factor that affects the transmitting quality. The mutual coupling factor $K$ can be calculated from (2). As a result, the received signals at the near end or far end can be calculated from (3)–(5):

\[
\rho = \frac{V_{\text{ref}}}{V_{\text{in}}} = \frac{(Z_t - Z_0)}{(Z_t + Z_0)} \tag{1}
\]

\[
K = \frac{L_{12}}{\sqrt{L_{11}L_{22}}} \tag{2}
\]

\[
V_x = V_{\text{crosstalk}} \left[1 + \frac{(Z_t - Z_0)}{(Z_t + Z_0)}\right] \tag{3}
\]

\[
\text{NEXT : } V_{\text{crosstalk}} = \frac{V_{\text{input}}}{4} \left(\frac{C_{12}}{C_{11}} + \frac{L_{12}}{L_{11}}\right) \tag{4}
\]

\[
\text{FEXT : } V_{\text{crosstalk}} = \frac{V_{\text{input}}}{2T_e} \left(\frac{C_{12}}{C_{11}} - \frac{L_{12}}{L_{11}}\right) \tag{5}
\]

where $V_{\text{ref}}$ is the reflected voltage value, $V_{\text{in}}$ is the input voltage value, $Z_0$ is the trace characteristic impedance, and $Z_t$ is the termination impedance. $L_{12}$ and $C_{12}$ are mutual inductance and mutual capacitance, $L_{11}$ and $L_{22}$ are self inductance, and $C_{11}$ and $C_{22}$ are self capacitance. $X$ is trace length, $T_e$ is edge rate, NEXT means the proximal, and FEXT means the distal.

From above analysis, the received signal waveforms are affected by various factors: the signal frequency, rising/falling edge, trace impedance, termination, crosstalk etc.

2.3 Two Time-domain Flow Comparison

In order to find out which flow can be used for quick post-layout simulation in time domain, Speed2000 and PowerSI/Hspice flows are compared for this FPGA development system. Fig. 5 shows a DQ simulation result at the SDRAM receiver side for the write operation. It can be seen that for all fast, typical, and slow corners, the waveforms from two flows are all correlated very well; the only small difference is that Speed2000 has more ringing and more fluctuation by considering the simultaneous switch noise (SSN) effect.

From the simulation setup and accuracy point of view, the PowerSI/Hspice flow has following positives: PowerSI is very efficient, and the interconnection performance and potential layout risks can be easily judged from the model; Hspice is also very efficient for both pre-layout and post-layout simulation, smart for transient data transaction, better in simulation convergence, very convenient for future result post-processing, and easy to sweep different corners to get the final solution space. The negatives include that the engineer needs more time to handle two tools and it is not intuitive to set probe observations. But the Speed2000 flow has these positives: it is able to obtain the solution by using one tool and easily for setup probe observations, which can probe arbitrary voltage and current waveforms on PCB, consider the SSN effect from other signals or power fluctuations, and get the crosstalk effect easily. The negatives of Speed2000 include that it is time consuming, it needs high-end computer to setup the mesh matrix, and it is not easy for sweeping parameters to find the solution space.

Fig. 5. DQ Simulation results of fast/typical/slow corner.

Fig. 6. ADD (A0) measurement.
3. Lab Measurement

The Tektronix oscilloscope (TDS7404) is used for the DDR3 waveform measurement. The scope is 4 GHz bandwidth with a 20 GS/s real-time sampling rate. Due to PCB test-point limitations, not every signal can be measured by the scope. Below are several signal waveforms measured in lab and compared with simulation, as shown in Fig. 6 (a) and (b) (ADD), Fig. 7 (a) and (b) (CLK), Fig. 8 (a) and (b) (DQ read), Fig. 9 (a) and (b) (DQS read), Fig. 10 (a) and (b) (DQ write). The peak-to-peak signal voltages are compared in Fig. 11. If good probe observations are designed, the correlation results can be better.

From above simulation and measurement comparisons, it is obvious that the PowerSI/Hspice flow can predict the real DDR3 performance very accurately and quickly, thus this flow is highly recommended for quick system-level DDR3 signal integrity simulation.
4. Conclusions

The current short time-to-market design needs quick system-level DDR3 SI simulation to find out the potential risks before system tape-out. The time-domain simulation results from two flows are compared, which are correlated very well. The simulation results are also verified with the lab measurement. The results show PowerSI and Hspice are a good tool combination for quick system-level DDR3 SI simulation.

References


